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Designing a high speed-low power carry select adder circuit using carbon nano tubes based on field effect transistors

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ABSTRACT

The purpose of this study is designing a carry select adder using carbon nano tubes based field effect transistors. As the main focus of VLSI circuit design is designing low power and high speed circuits, various methods have been introduced and developed to obtain this goal. In this study power consumption is reduced as much as possible utilizing nano scale transistors and decreasing supply voltage. To evaluate the proposed method CSA full adder is implemented as a case study. Considering different technologies CNTFET is selected for our design due to its advantages over its counterparts. Simulations are performed in HSPICE environment. Simulation results revealed that the proposed method is able to significantly decrease power, delay and power delay production.

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1. Introduction

The need for collecting, processing and storing data is increasing as a result of recent developments and progress in science and technology. In 1965 Moore, senior member of Intel, predicted that the number of transistors used in a single chip will be twice in each 18-month period while the die size will be halved; however, decrease of transistor size has consequences which may affect proper design of electronic circuits. The drawbacks of shrinking size of transistors are thin gate oxide (less than 1nm) which decreases control over gate of transistor, short channel effects and increase in leakage currents. Therefore, new technology and methods must be employed to design efficient nano-scale structures. In 1991, nano tubes were discovered. They were called multiple wall carbon nano tubes whose internal structure was similar to nested tubes. Two years later the same team built the first single wall nano tube with the same structure and characteristics. These tubes were very long and thin. The length of these tubes is usually much more than their diameter (they may differ thousand orders of magnitude). Carbon nano tubes provide designers with a specific material with incredible features consisting of low power consumption, high speed switching and short delay. So far, various full adders have been designed each of which has its pros and cons. Smaller number of transistors decreases die area and power consumptions; nevertheless, these are achieved at the expense of longer delay. One of the first full adders was a structure proposed in Navi et al. (2008) with 24 transistors. The next introduced structure was a 26-transistor symmetric circuit (Kavehei et al., 2008). Though power consumption of the former is less than the latter, it suffers from delay which is due to the fact that sum output should wait for the output. CPL full adder (Soudris et al., 2010) utilizes 18 transistors including NMOS pass transistors. In Chang et al. (2005) a variation of CPL called DPL is introduced using 24 transistors. The problem of CPL was that all of its output currents could not be seen in the output; thus, DPL was designed using PMOS transistor to address this issue. NCELL and HYBRID full adders were next generations implemented based on XOR/XNOR circuits. Hybrid full adder consist of 26 transistors and it has higher speed and lower delay value while it suffers from high power consumption (Shoarinejad et al., 2003; Goel et al., 2004). NCELL full adder includes 14 transistors and its sum output is not a full swing signal. N10T full adder designed in CMOS technology is composed of 10 transistors which leads to higher efficiency and smaller size. Finally, the full adder shown in Fig. 1 is designed in CMOS technology with 32nm channel length and 0.9V supply voltage including 24 transistors. The parameters of this full adder are presented in Table 1.

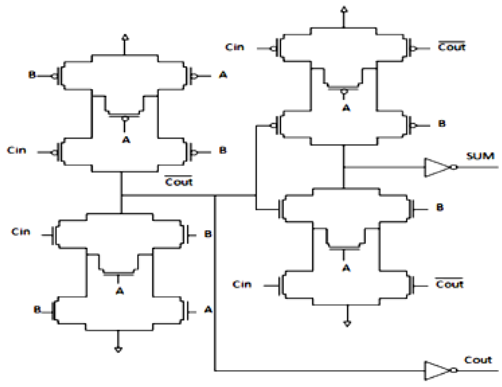

Fig. 1. Full adder circuit.

Table 1
Parameters of the circuit shown in Fig. 1.

Full Adder, CMOS-tech V_{DD} = 0.9v , L=32nm	
Power(w)	142E-9
Delay(s)	75E-9
PDP(s.w)	4.544E-15

The circuit depicted in Fig. 1 is designed using CNT based FETs with 32nm channel, 0.9 V supply voltage and three tubes. The schematic of circuit and its parameters could be found in Fig. 2 and Table 2, respectively.

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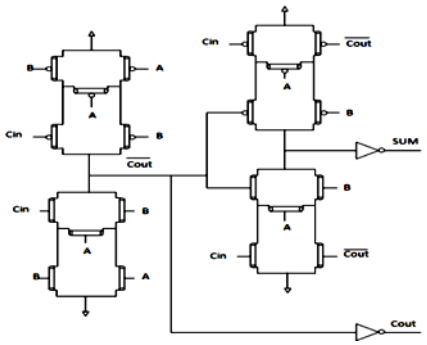

Fig. 2. Implementation of Fig. 1 circuit using CNTFET.

Table 2
Parameters of the circuit shown in Fig. 2.

Full Adder, CNT-Nano tech V_{pp} = 0.9v , L=32nm , Tubes =3	
Power(w)	9.05E-9
Delay(s)	5.17E-11
PDP(s.w)	4.68E-19

Shortcomings of CMOS transistors encouraged designers to exploit carbon nano tubes for digital circuit design. Lower power and higher speed make CNTFETs a promising alternative for CMOS technology. A variety of full adder circuits have been designed using CNTFETs (Amelifard et al., 2005). Since full adders are one of the most important blocks of digital circuits, optimizing their structure considerably improves output parameters of digital circuits.

In this paper, a CSA full adder is designed and simulated with 32nm CMOS technology with 0.9V supply. Afterwards, the same circuit is designed and simulated using CNTFETs with 32nm channel length, 0.9V supply voltage and three tubes. The diameter of nano tube is considered to be 1nm and both simulations are performed in T=27 ˚C.

2. Carbon nano tubes

The primary classification of carbon nano tubes is based on number of walls and concentric cylinders rolled up to form the tube. Based on this, CNTs are divided into two groups, SWCNT and MWCNT. If the nano tube is composed of one graphite tube it is called single walled CNT; otherwise, if it includes several concentric tubes it is called multi walled CNT. MWCNTs might be assumed as several single walled CNTs which are nested within one another (Fig. 3).

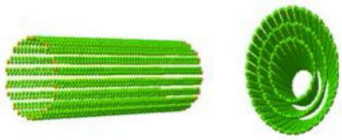

Fig. 3. Single walled and multi walled CNTs.

To obtain better understanding of SWCNT, imagine that they are achieved through rolling up a graphene sheet. Tube structure of SWCNT could be described using chiral vector

$$\vec{C}_h = n\vec{a}_1 + m\vec{a}_2 \quad (1)$$

where n and m are integer values demonstrating Chirality of the tube and a_1 and a_2 are constant vectors of graphene lattice. Fig. 4 depicts a schematic of chiral vectors of SWCNT.

Single walled nano tubes are divided into three essential groups based on carbon atoms arrangement; armchair and chiral (or asymmetric) which have metal properties and zigzag which has semiconductor properties. Metal or semiconductor characteristics are determined according to the arrangement of atoms and their angle along nano tube (Fig. 5). This is known as Chirality vector which is a prominent characteristic in CNT design. Using m and n it could be determined whether the nano tube is metallic or semiconducting. If two numbers are equal or their difference is a multiple of three, nano tube would be conductor and it would be semi-conductor, otherwise.

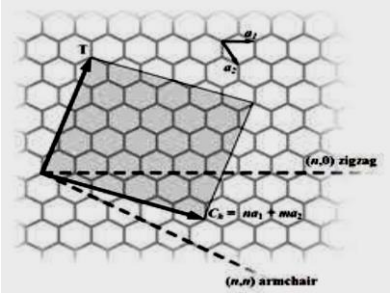

Fig 4. Schematic of SWCNT chiral vectors.

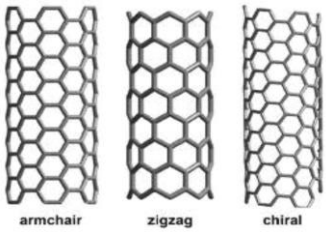

Fig. 5. Classification of nano tubes based on the direction of rolling graphene sheet.

3. CNT based FETs (CNTFETS)

As mentioned before a carbon nano tube can be considered as a single graphene sheet which is rolled up to a tube. The nano tube demonstrates semi-conductance or conductance characteristics in accordance with rolling direction. Metallic carbon nano tubes might be used as interconnects in integrated circuits while semiconducting ones might be utilized as CNTFET channels. These transistors are considerably fast as they benefits from electron ballistic transport through a low resistance path.

Three types of CNTFETS have been proposed including SN-CNTFET, CNTFET-T and MOSFET-Like CNTFET among which MOSFET-Like CNTFET is the most suitable one for designing CMOS based circuits owing to its inherent characteristics and more proper transistor structure. Fig. 6 demonstrates the structure of a MOSFEt-Like CNTFET.

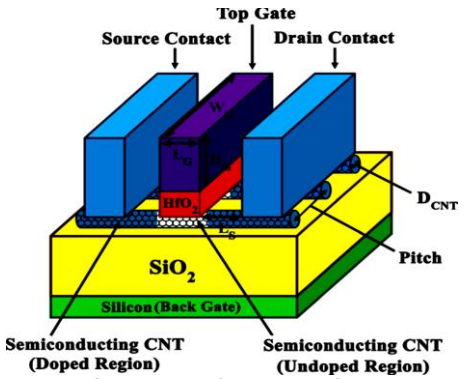

Fig. 6. The structure of a MOSFET-Like CNTFET.

Threshold voltage of CNTFET might be considered as first order approximation of the half of band gap according to Eq. 2.

$$v_{th} \approx \frac{E_{bg}}{2e} = \frac{\sqrt{3}}{3}\frac{aV_\pi}{eD_{CNT}} \approx \frac{0.436}{D_{CNT}(nm)} \quad (2)$$

where e is unit electron charge, E_{bg} is energy gap, a≈0/249nm is the distance between two carbon atoms, $V_\pi \approx 3.033$ is the carbon bond energy and DCNT is the diameter of CNT. According to the Eq. 2, threshold voltage of CNT based transistors is proportional

to inverse of carbon nano tubes diameter. The diameter of these nano tubes could be obtained via Eq. 3.

$$D_{CNT} = \frac{a\sqrt{(n^2+nm+m^2)}}{\pi} \approx 0.0783\sqrt{(n^2+nm+m^2)} \quad (3)$$

For example the diameter of a nano tube with (nm)=(29.0) equals 2.27nm and so threshold voltage is 0.192V. According to equations 2 and 3 the threshold voltage is inversely proportional to the nano tube diameter. To illustrate this characteristic a simple circuit illustrated in Fig. 7 is simulated. In this simulation CNT diameter is changed while all other parameters are considered to be constant. The results are demonstrated in Fig. 8.

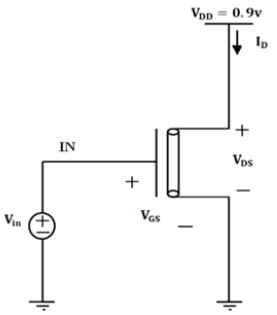

Fig. 7. Simple CNTFET based circuit.

CNTFETs have several advantages including high conductance, better threshold voltage, good sub threshold slope, high mobility, ballistic transport, high current density, low power and low delay. As mentioned before the behavior of CNTFET is very similar to CMOS and ID current increases when diameter or the number of tubes are raised. Figs. 9 and 10 illustrate these dependencies for the circuit of Fig. 7. Supply voltage is assumed to be 0.9V for this simulation.

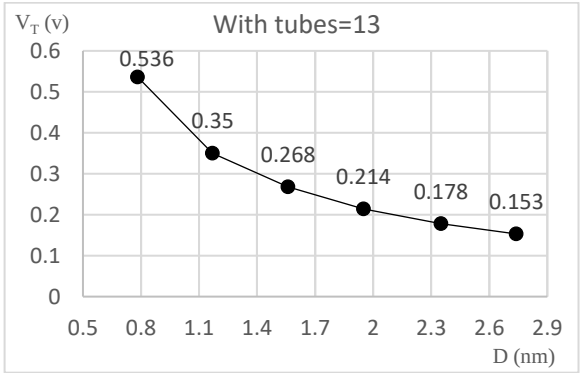

Fig. 8. Variations of threshold voltage vs nano tube diameter.

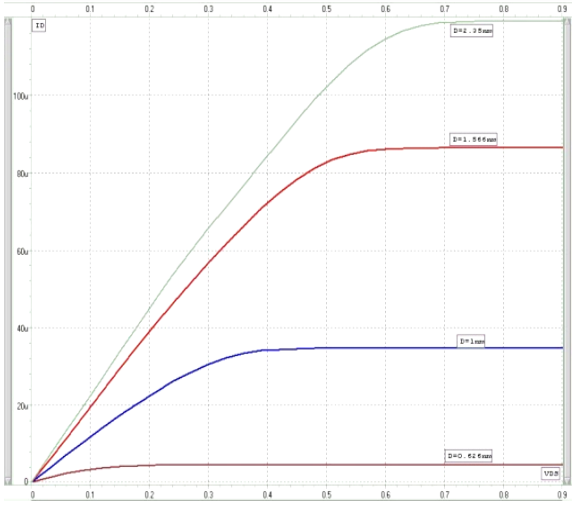

Fig. 9. Variations of tube current (ID) vs nano tube diameter (D).

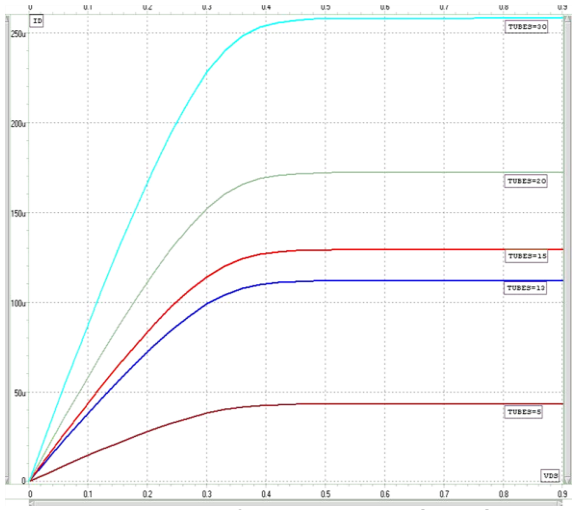

Fig. 10. Variations of ID vs variations in tube number.

In contrast, delay increases when tube diameter or the number of tubes increases. Figs. 11 and 12 demonstrate how delay is affected by variations in diameter and number of tubes.

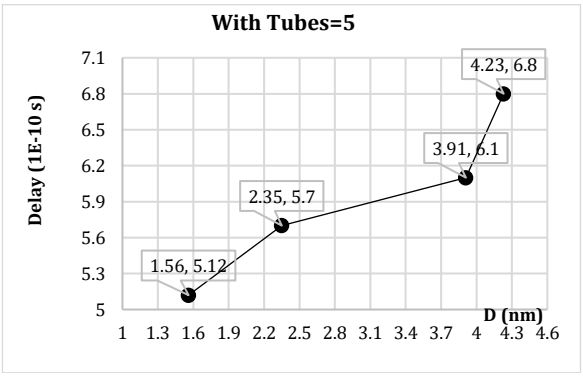

Fig. 11. Variations of propagation delay vs nano tube diameter variations.

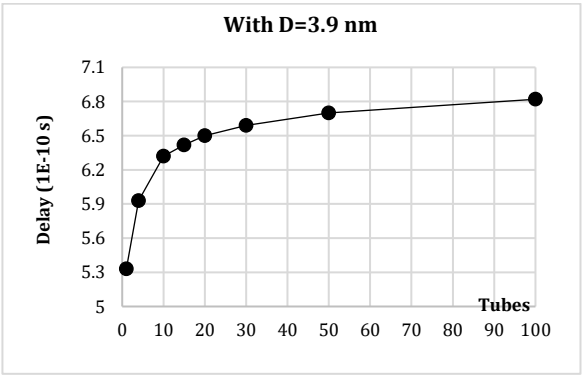

Fig. 12. Variations in propagation delay vs number of tubes.

Power consumption of CNTFETs is significantly lower than other technologies; however, it increases when diameter or number of tubes increase. Figs. 13 and 14 demonstrate how power consumption changes in case of variations in these two parameters.

4. CSA full adder using CNT based FETs

In this paper a CSA full adder is simulated and modified. It was previously proposed in Hiremath (2014) with 180nm CMOS technology and 1.8V supply. Fig. 15 depicts the schematic of the circuit. The simulation results could be found in Table 3. Full adders are implemented using Eq. 4.

$$SUM=A\oplus B\oplus Cin \quad (4)$$

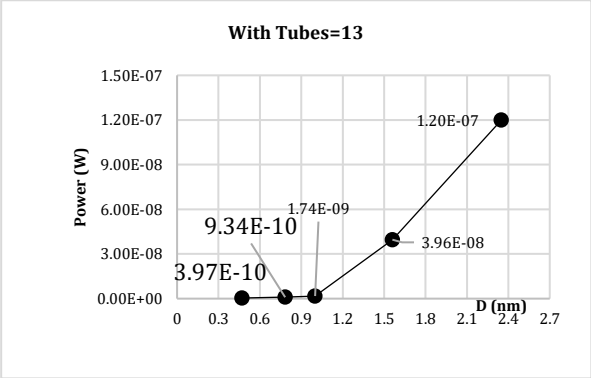

Fig. 13. Power consumption vs number of tubes.

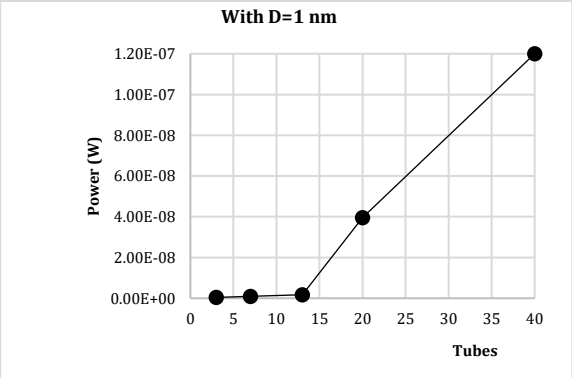

Fig. 14. Power consumption vs nano tube diameter.

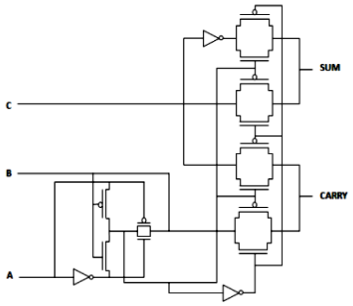

Fig. 15. CSA full adder implemented in CMOS technology.

Table 3
Simulation results of Fig. 15 (Hiremath, 2014).

Full Adder, V_{DD} = 1.8v L=180nm	
Power (w)	4.7E-6
Delay (s)	98.7E-12
PDP (s.w)	4.638E-16

In this paper, first off, the circuit shown in Fig. 15 is simulated in 32nm CMOS technology with 0.9V supply voltage utilizing HSPICE 2010. The library model used for our simulation is the model presented by Stanford University in 2008. As can be seen, 18 transistors are used for the design. Capacitors and resistors are avoided as they adversely affect delay, power and power delay production (PDP). Moreover, full swing is provided in output of the circuit. Simulation results are included in Table 4.

Table 4
Simulation results for circuit shown in Fig. 15 (32nm technology with 0.9V supply voltage).

Full Adder (Hiremath, 2014), proposed Design CMOS- Nano tech V_{DD} = 0.9v , L=32nm Proposed CMOS (Nano tech)		
Power (w)	Delay(s)	PDP (s.w)
144E-9	45E-12	64.8E-19

Fig. 16 shows the proposed CSA full adder. In fact, it is a new design of the circuit in Fig. 15 using CNTFETs with 32nm channel length and 0.9V supply voltage. There are three nano tubes, diameter is 1 nm and the temperature is assumed to be 27 degrees. HSPICE 2010 and the model provided by Stanford University are exploited for simulations.

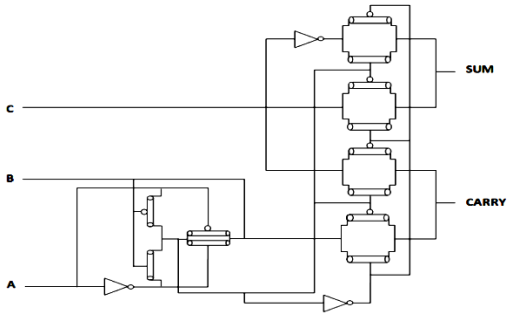

Fig. 16. The proposed CSA full adder based on CNTFETs.

Fig. 17 shows output waveforms for applied input pulses. Simulation results are also provided in Table 5.

5. Simulation results and comparison

Table 6 includes simulation results of different tested circuits as well as the proposed structure for two technologies. Figs. 18-20 illustrate delay, PDP, and power of simulated structures (the title of each bar shows the reference number in which the design is introduced as used in Table 6).

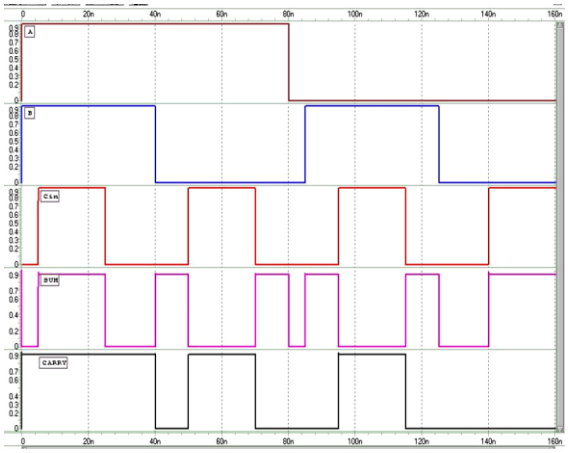

Fig. 17. Output waveforms of CSA full adder designed using CNTFETs (pulse inputs are considered).

Table 5
Simulation results of the full adder circuit for pulse inputs shown in Fig. 17.

Full Adder (Hiremath, 2014), proposed Design, CNT(Nano tech) V_{DD} = 0.9v , L=32nm , Tubes=3 , D=1nm		
Power (w)	Delay (s)	PDP (s.w)
6E-9	12E-12	72E-21

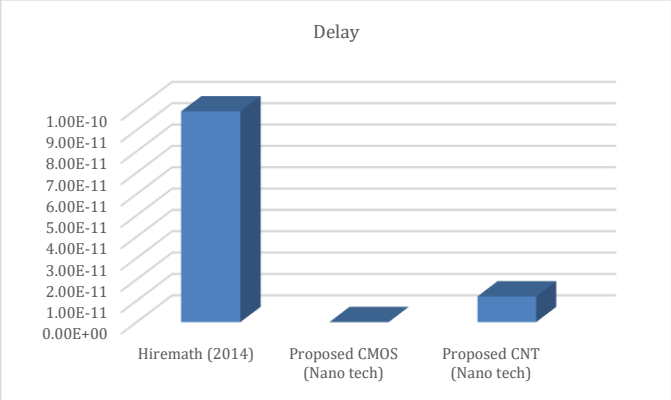

Fig. 18. Delay comparison.

Table 6
Simulation results for the proposed structure and other circuits (power, delay and PDP).

Design	Power(w)	Delay(s)	PDP(s.w)
Hiremath (2014)	4.7E-06	98.7E-12	4.638E-16
Proposed CMOS (Nano tech)	144E-9	45 E-12	64.8E-19
Proposed CNT (Nano tech)	6E-9	12E-12	72E-21

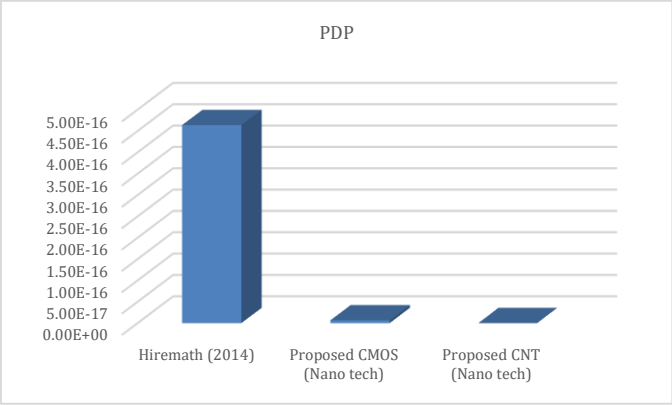

Fig. 19. PDP comparison for different structures in Table 6.

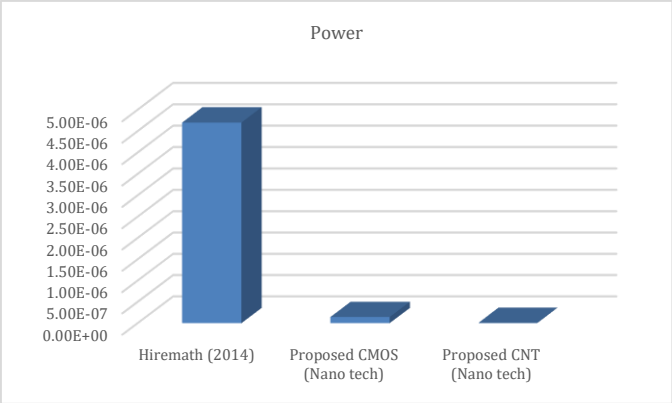

Fig. 20. Power comparison.

6. Conclusion

In this paper CNTFETs was proposed to improve delay, power and PDP of digital circuits. As a result of these improvements speed of the circuit also increases. The proposed design (CSA full adder) was firstly implemented in 32nm CMOS technology with 0.9V supply voltage exploiting HSPICE 2010. Then, the same structure was implemented using CNTFETs with 32nm channel length and 0.9V supply. Number of tubes and their diameter was considered three and 1nm, respectively. Simulation temperature was set to 27 ˚C.

Comparing simulation results for two technologies in similar conditions revealed that power, delay and PDP considerably decreases when CNTFET is used. It might be concluded that the proposed scheme is superior to previous structures and the same structure in CMOS technology.

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